Accelerate Your Time-to-Mission™

Digital to Analog
DA1
Function Module

MODULE MANUAL

Revision History

Revision	Revision Date	Description	Author
A	2/1/2018	Initial release	SL
A1	2/26/2018	ECO C05384 fixes to manual consistency issues	SL
A2	5/21/2018	ECO C05614 update to output specification and range and polarity register to improve clarity	SL
A3	8/15/2018	ECO C05798, correction to wrap voltage.	SL

Table of Contents

Introduction

This module manual provides information about the North Atlantic Industries, Inc. (NAI) Digital-to-Analog Function Module: DA1. This module is compatible with all NAI Generation 5 motherboards.

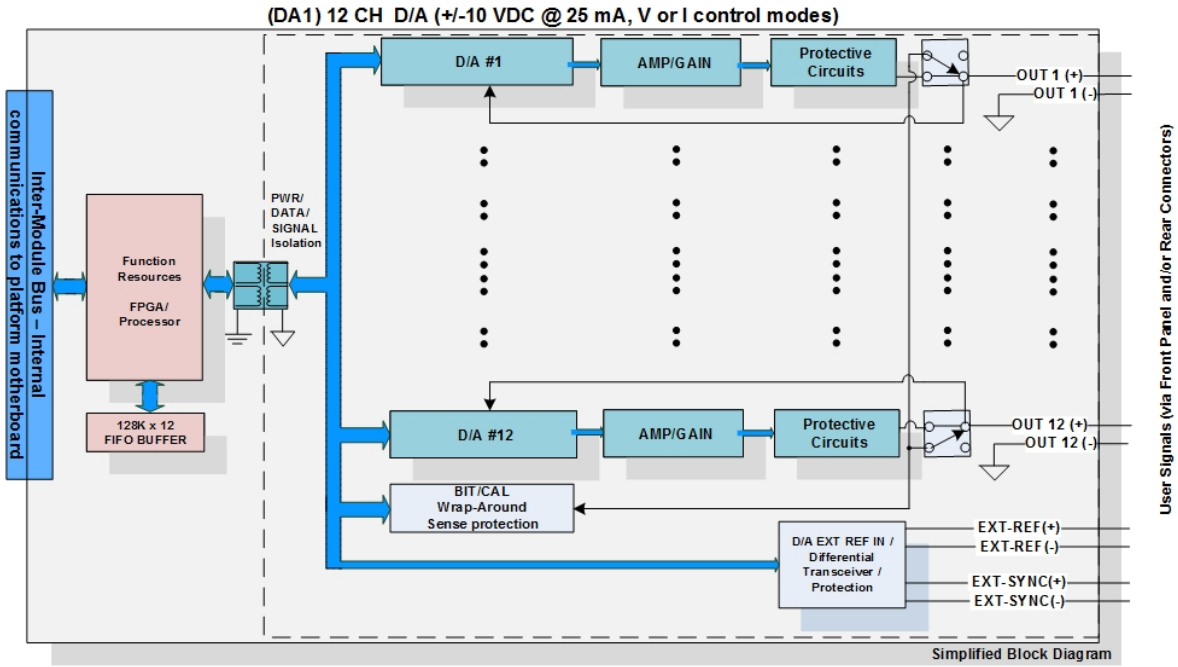
Digital-to-Analog (D/A) module DA1 provides 12 independent D/A output channels with a full-scale range of 0 to ±10 VDC (V-control mode) or 0 to ±25 mA (I-control mode). Linearity/accuracy is ±0.05% FS range over temperature. The DA1 provides either voltage or current control loop modes, which are programmable for the particular application. The DA1 module also provides external trigger/synchronization signal (RS-422/485) capability (pending), which provides/accepts a trigger signal to/from other module(s).

Features

- High-quality D/A conversion, 16-Bit/channel
- Designed to meet the testing requirements of IEC 801-2 Level 2
- Continuous background BIT
- External trigger/synchronization
- Automatic shutdown protection with the results displayed in a status word
- Extended D/A FIFO buffering capabilities

Specifications

Module DA1 – 12-Channel Digital-to-Analog (±10.0 VDC or ±25mA)



Resolution:	16-bit/channel for either voltage (V) or current (I) command modes.
Output Format:	Single-ended
Output Range:	±10 VDC, ±5 VDC, ±2.5 VDC, ±1.25 VDC (V-control mode bipolar) or 0 to10 VDC, 0 to 5 VDC, 0 to 2.5 VDC, 0 to 1.25 VDC (V-control mode unipolar). 0 to ±25 mA (I-control mode, bipolar only)
Output Impedance:	< 1 Ω
System Protection:	Output is set to 0 V at reset or Power-On.
Linearity Error:	±0.05% FS range over temperature (Voltage mode) ±0.1% FS range @ 25º C; derates linearly to ±0.2% FS range at -40 ºC & 85 ºC (Current mode)
Offset Error:	±5 mV / ±12.5 µA
Gain Error:	±0.03% FS range
Settling Time:	10 µs typical (15 µs max.)
Data Buffer:	See Operations Manual for details.
Load:	Can drive a capacitive load of 0.1 µF, 25 mA/CH max. (Source or Sink). Short circuit protected. When current exceeds 25 mA for any channel, for > 50 ms, that channel is set to 0 V (mA) and a flag is set.
Update Rate:	5 µs per channel
External Sync: (pending)	Module is provided with RS-485/422 transceiver for external channel output triggering and/or synchronization capabilities (provides or accepts trigger signal from other module(s).
ESD Protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4 kV transient with a peak current of 7.5 A and a time constant of approximately 60 ns).
Power:	5 VDC @ 300 mA typical (est.); ±12 VDC @ 200 mA (est. quiescent) Add 2 mA per 1 mA load per channel.
Ground:	All channel returns (CH-Lo (-)) are common, but are isolated (250 Vpeak) from system ground
Weight:	1.5 oz. (42 g)

Specifications are subject to change without notice.

Principle of Operation

In addition to the functions and features already described, each module includes extensive background BIT/diagnostics that run in the background in normal operation without user intervention. In addition to output signal read-back (wrap) capabilities, overloaded outputs will be detected with automatic channel shutdown protection, with the results displayed in a status word. The modules also include D/A FIFO Buffering for greater control of the output voltage and signal data. The FIFO D/A buffer will accept, store and output the voltage (and/or current) commands, once enabled and triggered, for applications requiring simulation of waveform generation; single or periodic (pending). The output data command word is formatted as a percentage of the full scale (FS) range selection, which allows maximum resolution and accuracy at lower voltage ranges.

Built-In Test (BIT)/Diagnostic Capability

Two different tests, one online (D2) and one offline (D3), may be selected:

The **online (D2)** test initiates automatic background BIT testing, where each channel is checked to a test accuracy of 0.2% FS and monitored for shorted output. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

The **offline (D3)** test uses an internal A/D that measures all D/A channels while they remain connected to the I/O and cycle through a number of signal levels. Each channel will be checked to a test accuracy of 0.2% FS. Test cycle is completed within 45 seconds and results can be read from the Status registers when D3 changes from **1** to **0**. The test can be stopped at any time. This test requires no user programming and can be enabled or disabled via the bus.

WARNING

D/A Outputs are active during D3 test. Check connected loads for interaction. D/A Overcurrent (short circuit) monitoring is disabled during D3 testing.

Note

If DA1 is set for Current Mode, and there is no load connected, BIT might be triggered.

Register Descriptions

The register descriptions provide the register name, Register Offset, Type, Data Range, Read or Write information, Initialized Value, a description of the function and, in most cases, a data table.

Set D/A Data

Function: Sets each channel for either unipolar or bipolar mode.

Type: binary word (16-bit)

Data Range: Unipolar: 0 to 0x0000 FFFF; Bipolar: 0xFFFF 8000 to 0x0000 7FFF

Read/Write: R/W

Initialized Value: 0x0000 0000

Operational Settings: Two's complement format for bipolar mode. See Data Range values above for unipolar and bipolar modes.

Default: 0x0000 0000

Set D/A Data															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

Polarity & Range

Function: Sets input format for polarity and range for each channel.

Type: binary word

Data Range: NA

Read/Write: R/W

Initialized Value: 0x0000000

Operational Settings: Set the range using bits **D0**, **D1**, **D2** and **D3**. See table below.

Default: Bipolar

Notes: For bipolar/unipolar selection, program **D4** to **0** for unipolar or **1** for bipolar.

Polarity & Range															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**

Polarity	**Range**				**Mode**
Bit 4 (D4)	**Bit 3 (D3)**	**Bit 2 (D2)**	**Bit 1 (D1)**	**Bit 0 (D0)**	
0	0	0	0	0	Unipolar 10 VDC/±25 mA range
1	0	0	0	0	Bipolar 10 VDC/±25 mA range
0	0	0	0	1	Unipolar 5 VDC/±12.5 mA range
1	0	0	0	1	Bipolar 5 VDC/±12.5 mA range
0	0	0	1	0	Unipolar 2.5 VDC/±6.25 mA range
1	0	0	1	0	Bipolar 2.5 VDC/±6.25 mA range
0	0	0	1	1	Unipolar 1.25 VDC/±3.125 mA range
1	0	0	1	1	Bipolar 1.25 VDC/±3.125 mA range

Capacitor/Bandwidth Select

Function: Filters output to provide a smooth analog waveform for each channel.

Type: binary word

Data Range: NA

Read/Write: R/W

Initialized Value: 0x0000 0000

Operational Settings: 0x00=off (3.3us), 0x10=1500 pF (122us), 0x11=0.015 uF (1.32ms), 0x12=0.15 uF (11.2ms), 0x13=0.47 uF (21ms). See table below.

Default: 0x0000 0000

Notes: Set **D4** to **0** to Disable or **1** to Enable register. Set **D1** and **D0** (Bandwidth Select) as indicated above.

Capacitor/Bandwidth Select															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**

Polarity	**Range**				**Mode**
Bit 4 (D4)	**Bit 3 (D3)**	**Bit 2 (D2)**	**Bit 1 (D1)**	**Bit 0 (D0)**	
0	0	0	0	0	Disabled (3.3 µs)
1	0	0	0	0	Enabled 1500 pF (122 µs)
1	0	0	0	1	Enabled 0.015 µF (1.32 ms)
1	0	0	1	0	Enabled 0.15 µF (11.2 ms)
1	0	0	1	1	Enabled 0.47 µF (21 ms)

Wrap Voltage

Function: Used to read the measured output voltage.

Type: binary word (32-bit)

Data Range: 0xFFFF 8000 to 0x0000 7FFF

Read/Write: R

Initialized Value: 0x0000 0000

Operational Settings: Fixed in bipolar mode with no ranges - 0x7FFF= 13 V.

Default: 0x0000 0000

Wrap Voltage															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

Current Reading

Function: Reads current values of D/A outputs being delivered per channel. (Bipolar mode only.)
Type: binary word (32-bit)
Data Range: For bipolar mode: 0xFFFF 8000 to 0x0000 7FFF
Read/Write: R
Initialized Value: 0
Operational Settings: Fixed in bipolar mode with no ranges - 0x7FFF = 25 mA.
Default: 0x0000 0000

Current Reading															
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Trigger Control

Function: Starts/triggers FIFO when FIFO registers are enabled or writes D/A data that was previously written when the *Output Data Trigger* register is enabled. FIFO can be started/triggered by different sources.
Data Range: 0x0 to 0xFFF
Read/Write: R/W
Initialized Value: 0
Operational Settings: See the tables that follow for settings.
Default: Disabled Trigger

B[1..0]	Trigger Type
0	Continuous
1	Single Sample
2	X
3	X

X= Don't care

B[5..4]	Trigger Edge
0	Hardware Trigger - Positive Edge (Pending)
1	Hardware Trigger - Negative Edge (Pending)
2	Hardware Trigger - Either Edge (Pending)
3	Software Trigger

B8	Trigger Enable
0	Not Enabled / Stop Trigger
1	Enable Trigger

B[8..0]	Description
0x100	Use FIFO continuously once there is a positive edge on the Hardware Trigger
0x101	Use single FIFO sample once there is a positive edge on the Hardware Trigger
0x110	Use FIFO continuously once there is a negative edge on the Hardware Trigger
0x111	Use single FIFO sample once there is a negative edge on the Hardware Trigger
0x120	Use FIFO continuously once there is a positive or negative edge on the Hardware Trigger
0x121	Use single FIFO sample once there is a positive or negative edge on the Hardware Trigger
0x130	Use FIFO continuously once there is a Software Trigger
0x131	Use single FIFO sample once there is a Software Trigger
0x0XX	Disable Trigger (will stop FIFO from storing data if continuously running)

Output Data Trigger

Function: Sets up trigger control for D/A outputs for each channel.

Type: binary word (32-bit)

Data Range: 0 to 0x0000 0001

Read/Write: R

Initialized Value: 0

Operational Settings: D/A output voltages can be programmed to change only with a synchronizing trigger, or to constantly update, based on the settings of the register. **0** = Constant Update; **1** = Trigger. When in trigger mode, the trigger control register is used to set up what kind of trigger condition (hardware, software, which edge, etc.). Once that trigger condition is met, the data in the D/A data is updated. If in constant update mode, the D/A data is update immediately upon writing the data.

Default: 0

Output Data Trigger																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Constant
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	Constant

Software Trigger

Function: Software trigger is used to kick start the FIFO buffer and the output of data or the output of the Set D/A Data depending if the FIFO buffer control is enabled or not.

Data Range: 0 to 0x0000 0001

Read/Write: R/W

Initialized Value: 0

Operational Settings: In order to use this operation, the *Trigger Control* register must be set up as described in the *Trigger Control* register and the *Output Data Trigger* register must be enabled. Write a **1** to trigger FIFO output for each channel (bitmapped for each channel).

Default: Not Triggered

DA Sample Rate

Function: Single 32-bit register that sets the desired sample rate for all channels.
Data Range: 0x186A0 to 0x61A80
Read/Write: R/W
Initialized Value: 400 kHz
Operational Settings: Sets sampling rate for all channels. Range is 100 kHz to 400 kHz.
Default: Initialized to 400 kHz sampling rate per channel

DA Sample Rate																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	LSB=1 Hz=DATA BIT=D

VI Control

Function: Sets each channel for voltage mode or current mode.
Register Offset(s): 0x1280
Data Range: 0 to 0xFFFF
Read/Write: R/W
Initialized Value: 0
Operational Settings: Set bit to **1** for Current mode and **0** for Voltage mode.
Default: Voltage mode

Test Enable

Function: Enables D0, D2 and D3 BIT testing
Register Offset(s) Ch1-Ch12: 0x0248
Data Range: NA
Read/Write: R/W
Initialized Value: 0
Operational Settings: 0 = Disabled; **1** = Enabled
Default: 0

FIFO Buffer Data

Function: Data is written to this register and can be retrieved, one word at a time (16-bits), in the Register Offset(s) Ch1-Ch12 addresses listed below. Buffer can be completely emptied when triggered.

Data Range: For bipolar mode: 7FFFh = +FS, 8000h = -FS. For unipolar mode, range is from 0h to FFFFh = FS.

Read/Write: R/W

Initialized Value: 0

Operational Settings: The data is presented depending upon how the *Set D/A Data* register is set, (either unipolar or bipolar). Data is held in FIFO until triggered.

Default: Nothing in FIFO

FIFO Word Count

Function: This is a counter that reports the number of 16-bit words stored in the FIFO buffer.

Type: binary word (32-bit)

Data Range: 0 to 0x001F FFFF

Read/Write: R

Initialized Value: 0

Operational Settings: Every time a *FIFO Buffer Data* register word is sent out after triggering, its corresponding *FIFO Word Count* register will be decremented by one. The maximum number of words that can be stored in the FIFO is 1 mega words (2 M pending).

Default: Nothing in FIFO (empty)

FIFO Buffer Clear

Function: Clears FIFO whenever clear memory is set or reset for the individual channel in the Register Offset Ch1-Ch12 addresses listed below.

Data Range: 0x0000 0000 to 0x0000 0001

Read/Write: R/W

Initialized Value: 0

Operational Settings: Any write operation will clear *FIFO Buffer Data* register.

Default: Not clearing

FIFO Empty Mark

Function: This register enables the user to set the limits for the “almost empty” status.

Type: binary word (32-bit)

Data Range: 0 to 0x001F FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: When the *FIFO Word Count* register is less than or equal to the value stored in the *FIFO Empty Mark* register, the “almost empty” bit (B0) of the *FIFO Status* register will be set. When the *Words in FIFO* counter is greater than the value stored in the register, the almost empty bit (B1) of the *FIFO Status* register will be reset.
Set = logical **1**
Reset = logical **0**
Default: Not set

FIFO Low Mark

Function: The FIFO Low Mark (low-threshold level) is used to set or reset the low limit bit (**B2**) of the individual *FIFO Status* register in the Register Offset Ch1-Ch12 addresses listed below.

Data Range: 0 to 0x001F FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: When the *FIFO Word Count* register is less than or equal than the value stored in the *FIFO Low Mark* register, the low limit bit (**B2**) of the *FIFO Status* register will be set. When the *FIFO Word Count* counter is greater than or equal to the value stored in the register, the low limit bit (**B2**) of the *FIFO Status* register will be reset.

Set = logical **1**

Reset = logical **0**

Default: Not set

FIFO High Mark

Function: The FIFO High Mark (hi-threshold level) is used to set the high limit bit (**B3**) of the individual channel *FIFO Status* register in the Register Offset Ch1-Ch12 addresses listed below.

Data Range: 0 to 0x001F FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: When the *FIFO Word Count* register is greater than or equal to the value stored in the *FIFO High Mark* register, the high limit bit (**B3**) of the *FIFO Status* register will be set. When the *FIFO Word Count* register is less than the value stored in the hi-threshold, the high limit bit (**B3**) of the *FIFO Status* register will be reset.
Set = logical **1**
Reset = logical **0**
Default: Not set

FIFO Full Mark

Function: This register enables the user to set the limits for the “almost full” status.

Data Range: 0 to 0x001F FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: When the *FIFO Word Count* register is greater than or equal to the value stored in the *FIFO Full* register, the almost full bit (**B4**) of the *FIFO Status* register will be set. When the *Words in FIFO* counter is less than the value stored in the register, the almost full bit (**B4**) of the *FIFO Status* register will be reset.
Set = logical **1**
Reset = logical **0**
Default: Not set

FIFO Buffer Control

Function: Enables the usage of the FIFO buffer and the FIFO mode.

B0	FIFO Enable
B1	Enable Repeat Mode (Pending)

Data Range: 0 to 0x000 000FF

Read/Write: R/W

Initialized Value: 0

Operational Settings: FIFO Enable (**B0**) enables using the FIFO registers as the source for output of data to the D/A converters. Enable Repeat Mode (**B1**) functionality is pending and will be implemented at a later date.

FIFO Buffer Control															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	**B1**	**B0**

Status and Interrupt Registers

The registers may be set for any or all channels and will latch if a transition is detected on a channel or channels. Each channel(s) will remain latched until the channel is cleared. Multiple channels may be cleared simultaneously, if desired. Each channel bit in the register is polled for a read status. Any subsequent channel(s) transition, if detected, will propagate through to be read (rolling-latch).

Once the status register has been read, the act of writing a **1** back to the applicable status register to any specific bit (channel) location (bit mapped per channel), will "clear" the bit (set the bit to **0**) if the actual interruptible event condition has cleared. If the interruptible condition "event" is still persistent while clearing, this may retrigger the interrupt.

There is a corresponding Interrupt Enable and vector associated with each "Latched" Status. Each status type may be "polled" (at any time), or is "interruptible" when interrupts are enabled and the associated Interrupt Service Routine (ISR) vectors are programmed accordingly. When programmed for "interruptible" status, interrupts are typically generated and flagged with the programmed vector available as data. The host or single board computer (SBC) typically services the interrupt by a general or specific ISR, which reads the (typically) unique programmed vector (identifier of which status generated the interrupt), reads the associated status register to determine which channel in the status register was "flagged" and then "clears" the status register. This essentially resets the interrupt mechanism, which is now ready to be triggered by the next status register detected event "flag". "Latched Status" will trigger on either "sense on edge" or "sense on level" based on the settings of the associated Set Edge/Level Interrupt register. Sense on "edge" requires a change from low to high state to trigger the status detection, while sense on "level" is independent of the previous state. Unless otherwise specified, all status or fault indications are bit set per channel.

BIT Dynamic Status

Function: Continuously reports the status of the Built In Self Tests.

Read/Write: R

Initialized Value: 0

Operational Settings: 0 = Normal; **1** = Non-compliant D/A conversion (outside 0.2% FS range accuracy spec).

Notes: BIT Status is part of background testing and the status register may be checked or polled at any given time.

BIT Dynamic Status															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Latched Status

Function: Latches high when there's a non-compliant status until cleared.

Read/Write: R/W

Initialized Value: 0

Operational Settings: 0 = Normal; **1** = Non-compliant D/A conversion (outside 0.2% FS range accuracy spec). Write a **1** to this register to clear status.

Notes: BIT Status is part of background testing and the status register may be checked or polled at any given time.

BIT Latched Status															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Interrupt Enable

Function: Sets the bit to enable interrupts for the corresponding channel.

Read/Write: R/W

Initialized Value: 0

Operational Settings: When enabled, a non-compliant channel will trigger an interrupt.

Default: 00h to disable all channels

BIT Interrupt Enable															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Set Edge/Level Interrupt

Function: When the *BIT Interrupt Enable* register is enabled, this register determines whether the interrupt will be generated for either “sense on edge” or “sense on level” event detection.

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to sense on level and a **0** to sense on edge.

Default: Sense on edge (**0**)

BIT Set Edge/Level Interrupt															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

FIFO Dynamic Status

Function: Checks the corresponding bit for a channel's FIFO Status. The *FIFO Dynamic Interrupt Status* register indicates the current condition of the FIFO buffer.

Type: binary word (32-bit)

Data Range: 0 to 0x0000 007F

Read/Write: R

Initialized Value: 0

Operational Settings: D0-**D6** is used to show the different conditions of the buffer.

Description		Configurable?
D0	Empty; 1 when FIFO Count = 0	No
D1	Almost Empty; 1 when FIFO Count <= AE register	Yes
D2	Low Watermark; 1 when FIFO Count <= LWM register	Yes
D3	High Watermark; 1 when FIFO Count >= HWM register	Yes
D4	Almost Full; 1 when FIFO Count >= AF register	Yes
D5	Full; 1 when FIFO Count = 1 Mega Words (2 M pending)	No
D6	Sample Done; 1 when FIFO Count "FIFO Buffer Size" register	Yes

FIFO Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

FIFO Latched Status

Function: Checks the corresponding bit for a channel's FIFO Status. The *FIFO Latched Interrupt Status* register maintains the last condition of the FIFO buffer, until cleared.

Type: binary word (32-bit)

Data Range: 0 to 0x0000 007F

Read/Write: R/W

Initialized Value: 0

Operational Settings: D0-**D6** is used to show the different conditions of the buffer. Write a **1** to this register to clear status.

Description		Configurable?
D0	Empty; 1 when FIFO Count = 0	No
D1	Almost Empty; 1 when FIFO Count <= AE register	Yes
D2	Low Watermark; 1 when FIFO Count <= LWM register	Yes
D3	High Watermark; 1 when FIFO Count >= HWM register	Yes
D4	Almost Full; 1 when FIFO Count >= AF register	Yes
D5	Full; 1 when FIFO Count = 1 Mega Words (2 M pending)	No
D6	Sample Done; 1 when FIFO Count "FIFO Buffer Size" register	Yes

FIFO Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

FIFO Status Interrupt Enable

Function: Sets the corresponding channel bit to enable an interrupt for each of the conditions indicated in the FIFO Status register (D0..D6).

Data Range: 0 to 0x7FFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: When enabled, an interrupt will be generated for each of the following conditions. Each channel may be set for a different condition.

Description		Configurable?
D0	Empty; 1 when FIFO Count = 0	No
D1	Almost Empty; 1 when FIFO Count <= AE register	Yes
D2	Low Watermark; 1 when FIFO Count <= LWM register	Yes
D3	High Watermark; 1 when FIFO Count >= HWM register	Yes
D4	Almost Full; 1 when FIFO Count >= AF register	Yes
D5	Full; 1 when FIFO Count = 1 Mega Words (2 M pending)	No
D6	Sample Done; 1 when FIFO Count "FIFO Buffer Size" register	Yes

FIFO Status Interrupt Enable															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

FIFO Set Edge/Level Interrupt

Function: When the *FIFO Mask Status Interrupt Enable* register is enabled, this register determines whether the interrupt will be generated for either “sense on edge” or “sense on level” event detection.

Data Range: 0 to 0x7FFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to sense on level and a **0** to sense on edge.

Default: Sense on edge (**0**)

FIFO Set Edge/Level Interrupt															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Overcurrent Dynamic Status

Function: Continuously reports the overcurrent status of each channel.

Read/Write: R

Initialized Value: 0

Operational Settings: 0 = Normal; **1** = Overcurrent

Overcurrent Dynamic Status															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Overcurrent Latched Status

Function:

Latches high when an overcurrent condition occurs until cleared.

Read/Write: R/W

Initialized Value: 0

Operational Settings: 0 = Normal; **1** = Overcurrent. Write a **1** to this register to clear status.

Overcurrent Latched Status															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Overcurrent Interrupt Enable

Function: Sets the corresponding channel bit to enable an interrupt for an overcurrent condition as specified in the *Current Reading* register.

Read/Write: R/W

Initialized Value: 0

Operational Settings: When enabled, a non-compliant channel will trigger an interrupt.

Default: 00h to disable all channels

Overcurrent Interrupt Enable															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Overcurrent Set Edge/Level Interrupt

Function: When the *Overcurrent Mask Status Interrupt Enable* register is enabled, this register determines whether the interrupt will be generated for either “sense on edge” or “sense on level” event detection.

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to sense on level and a **0** to sense on edge.

Default: Sense on edge (**0**)

Overcurrent Set Edge/Level Interrupt															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Function Register Map

0x1000	Set D/A Data Ch. 1	R/W
0x1004	Set D/A Data Ch. 2	R/W
0x1008	Set D/A Data Ch. 3	R/W
0x100C	Set D/A Data Ch. 4	R/W
0x1010	Set D/A Data Ch. 5	R/W
0x1014	Set D/A Data Ch. 6	R/W
0x1018	Set D/A Data Ch. 7	R/W
0x101C	Set D/A Data Ch. 8	R/W
0x1020	Set D/A Data Ch. 9	R/W
0x1024	Set D/A Data Ch. 10	R/W
0x1028	Set D/A Data Ch. 11	R/W
0x102C	Set D/A Data Ch. 12	R/W

0x1080	Polarity & Range Ch.1 & 2	R/W
0x1084	Polarity & Range Ch.3 & 4	R/W
0x1088	Polarity & Range Ch.5 & 6	R/W
0x108C	Polarity & Range Ch.7 & 8	R/W
0x1090	Polarity & Range Ch.9 & 10	R/W
0x1094	Polarity & Range Ch.11 & 12	R/W
0x10C0	Capacitor/Bandwidth Select Ch.1 & 2	R/W
0x10C4	Capacitor/Bandwidth Select Ch.3 & 4	R/W
0x10C8	Capacitor/Bandwidth Select Ch.5 & 6	R/W
0x10CC	Capacitor/Bandwidth Select Ch.7 & 8	R/W
0x10D0	Capacitor/Bandwidth Select Ch.9 & 10	R/W
0x10D4	Capacitor/Bandwidth Select Ch.11 & 12	R/W

0x1100	Wrap Voltage Ch.1	R
0x1104	Wrap Voltage Ch.2	R
0x1108	Wrap Voltage Ch.3	R
0x110C	Wrap Voltage Ch.4	R
0x1110	Wrap Voltage Ch.5	R
0x1114	Wrap Voltage Ch.6	R
0x1118	Wrap Voltage Ch.7	R
0x111C	Wrap Voltage Ch.8	R
0x1120	Wrap Voltage Ch.9	R
0x1124	Wrap Voltage Ch.10	R
0x1128	Wrap Voltage Ch.11	R
0x112C	Wrap Voltage Ch.12	R

0x1180	Current Reading Ch. 1	R
0x1184	Current Reading Ch. 2	R
0x1188	Current Reading Ch. 3	R
0x118C	Current Reading Ch. 4	R
0x1190	Current Reading Ch. 5	R
0x1194	Current Reading Ch. 6	R
0x1198	Current Reading Ch. 7	R
0x119C	Current Reading Ch. 8	R
0x11A0	Current Reading Ch. 9	R
0x11A4	Current Reading Ch. 10	R
0x11A8	Current Reading Ch. 11	R
0x11AC	Current Reading Ch. 12	R

0x1200	Output Data Trigger Ch. 1	R/W
0x1204	Output Data Trigger Ch. 2	R/W
0x1208	Output Data Trigger Ch. 3	R/W
0x120C	Output Data Trigger Ch. 4	R/W
0x1210	Output Data Trigger Ch. 5	R/W
0x1214	Output Data Trigger Ch.6	R/W
0x1218	Output Data Trigger Ch.7	R/W
0x121C	Output Data Trigger Ch. 8	R/W
0x1220	Output Data Trigger Ch. 9	R/W
0x1224	Output Data Trigger Ch. 10	R/W
0x1228	Output Data Trigger Ch. 11	R/W
0x122C	Output Data Trigger Ch. 12	R/W

0x1380	FIFO Buffer Data Ch. 1	R/W
0x1384	FIFO Buffer Data Ch. 2	R/W
0x1388	FIFO Buffer Data Ch. 3	R/W
0x138C	FIFO Buffer Data Ch. 4	R/W
0x1390	FIFO Buffer Data Ch. 5	R/W
0x1394	FIFO Buffer Data Ch. 6	R/W
0x1398	FIFO Buffer Data Ch. 7	R/W
0x139C	FIFO Buffer Data Ch. 8	R/W
0x13A0	FIFO Buffer Data Ch. 9	R/W
0x13A4	FIFO Buffer Data Ch. 10	R/W
0x13A8	FIFO Buffer Data Ch. 11	R/W
0x13AC	FIFO Buffer Data Ch. 12	R/W

0x1400	FIFO Word Count Ch.1	R
0x1404	FIFO Word Count Ch.2	R
0x1408	FIFO Word Count Ch.3	R
0x140C	FIFO Word Count Ch.4	R
0x1410	FIFO Word Count Ch.5	R
0x1414	FIFO Word Count Ch.6	R
0x1418	FIFO Word Count Ch.7	R
0x141C	FIFO Word Count Ch.8	R
0x1420	FIFO Word Count Ch.9	R
0x1424	FIFO Word Count Ch.10	R
0x1428	FIFO Word Count Ch.11	R
0x142C	FIFO Word Count Ch.12	R

0x1480	FIFO Buffer Clear Ch.1	R/W
0x1484	FIFO Buffer Clear Ch.2	R/W
0x1488	FIFO Buffer Clear Ch.3	R/W
0x148C	FIFO Buffer Clear Ch.4	R/W
0x1490	FIFO Buffer Clear Ch.5	R/W
0x1494	FIFO Buffer Clear Ch.6	R/W
0x1498	FIFO Buffer Clear Ch.7	R/W
0x149C	FIFO Buffer Clear Ch.8	R/W
0x14A0	FIFO Buffer Clear Ch.9	R/W
0x14A4	FIFO Buffer Clear Ch.10	R/W
0x14A8	FIFO Buffer Clear Ch.11	R/W
0x14AC	FIFO Buffer Clear Ch.12	R/W

0x1500	FIFO E Mark Ch. 1	R/W
0x1504	FIFO E Mark Ch. 2	R/W
0x1508	FIFO E Mark Ch. 3	R/W
0x150C	FIFO E Mark Ch. 4	R/W
0x1510	FIFO E Mark Ch. 5	R/W
0x1514	FIFO E Mark Ch. 6	R/W
0x1518	FIFO E Mark Ch. 7	R/W
0x151C	FIFO E Mark Ch. 8	R/W
0x1520	FIFO E Mark Ch. 9	R/W
0x1524	FIFO E Mark Ch. 10	R/W
0x1528	FIFO E Mark Ch. 11	R/W
0x152C	FIFO E Mark Ch. 12	R/W

0x1580	FIFO Lo Mark Ch.1	R/W
0x1584	FIFO Lo Mark Ch.2	R/W
0x1588	FIFO Lo Mark Ch.3	R/W
0x158C	FIFO Lo Mark Ch.4	R/W
0x1590	FIFO Lo Mark Ch.5	R/W
0x1594	FIFO Lo Mark Ch.6	R/W
0x1598	FIFO Lo Mark Ch.7	R/W
0x159C	FIFO Lo Mark Ch.8	R/W
0x15A0	FIFO Lo Mark Ch.9	R/W
0x15A4	FIFO Lo Mark Ch.10	R/W
0x15A8	FIFO Lo Mark Ch.11	R/W
0x15AC	FIFO Lo Mark Ch.12	R/W

0x1600	FIFO Hi Mark Ch.1	R/W
0x1604	FIFO Hi Mark Ch.2	R/W
0x1608	FIFO Hi Mark Ch.3	R/W
0x160C	FIFO Hi Mark Ch.4	R/W
0x1610	FIFO Hi Mark Ch.5	R/W
0x1614	FIFO Hi Mark Ch.6	R/W
0x1618	FIFO Hi Mark Ch.7	R/W
0x161C	FIFO Hi Mark Ch.8	R/W
0x1620	FIFO Hi Mark Ch.9	R/W
0x1624	FIFO Hi Mark Ch.10	R/W
0x1628	FIFO Hi Mark Ch.11	R/W
0x162C	FIFO Hi Mark Ch.12	R/W

0x1680	FIFO F Mark Ch. 1	R/W
0x1684	FIFO F Mark Ch. 2	R/W
0x1688	FIFO F Mark Ch. 3	R/W
0x168C	FIFO F Mark Ch. 4	R/W
0x1690	FIFO F Mark Ch. 5	R/W
0x1694	FIFO F Mark Ch. 6	R/W
0x1698	FIFO F Mark Ch. 7	R/W
0x169C	FIFO F Mark Ch. 8	R/W
0x16A0	FIFO F Mark Ch. 9	R/W
0x16A4	FIFO F Mark Ch. 10	R/W
0x16A8	FIFO F Mark Ch. 11	R/W
0x16AC	FIFO F Mark Ch. 12	R/W

0x1880	FIFO Buffer Control Ch.1	R/W
0x1884	FIFO Buffer Control Ch.2	R/W
0x1888	FIFO Buffer Control Ch.3	R/W
0x188C	FIFO Buffer Control Ch.4	R/W
0x1890	FIFO Buffer Control Ch.5	R/W
0x1894	FIFO Buffer Control Ch.6	R/W
0x1898	FIFO Buffer Control Ch.7	R/W
0x189C	FIFO Buffer Control Ch.8	R/W
0x18A0	FIFO Buffer Control Ch.9	R/W
0x18A4	FIFO Buffer Control Ch.10	R/W
0x18A8	FIFO Buffer Control Ch.11	R/W
0x18AC	FIFO Buffer Control Ch.12	R/W

0x1280	VI Mode	R/W
0x1294	DA Sample Rate	R/W
0x129C	Software Trigger	R/W
0x0248	Test Enable	R/W

0x1900	Trig Control Ch.1	R/W
0x1904	Trig Control Ch.2	R/W
0x1908	Trig Control Ch.3	R/W
0x190C	Trig Control Ch.4	R/W
0x1910	Trig Control Ch.5	R/W
0x1914	Trig Control Ch.6	R/W
0x1918	Trig Control Ch.7	R/W
0x191C	Trig Control Ch.8	R/W
0x1920	Trig Control Ch.9	R/W
0x1924	Trig Control Ch.10	R/W
0x1928	Trig Control Ch.11	R/W
0x192C	Trig Control Ch.12	R/W

BIT

0x0800	Dynamic Status	R
0x0804	Latched Status	R/W
0x0808	Interrupt Enable	R/W
0x080C	Set Edge/Level Interrupt	R/W

FIFO Dynamic Status, FIFO Latched Status, FIFO Interrupt Enable, FIFO Set Edge/Level Interrupt

Ch. 1	0x0810	Dynamic Status	R	**Ch. 7**	0x0870	Dynamic Status	R
	0x0814	Latched Status	R/W		0x0874	Latched Status	R/W
	0x0818	Interrupt Enable	R/W		0x0878	Interrupt Enable	R/W
	0x081C	Set Edge/Level Interrupt	R/W		0x087C	Set Edge/Level Interrupt	R/W
Ch. 2	0x0820	Dynamic Status	R	**Ch. 8**	0x0880	Dynamic Status	R
	0x0824	Latched Status	R/W		0x0884	Latched Status	R/W
	0x0828	Interrupt Enable	R/W		0x0888	Interrupt Enable	R/W
	0x082C	Set Edge/Level Interrupt	R/W		0x088C	Set Edge/Level Interrupt	R/W
Ch. 3	0x0830	Dynamic Status	R	**Ch. 9**	0x0890	Dynamic Status	R
	0x0834	Latched Status	R/W		0x0894	Latched Status	R/W
	0x0838	Interrupt Enable	R/W		0x0898	Interrupt Enable	R/W
	0x083C	Set Edge/Level Interrupt	R/W		0x089C	Set Edge/Level Interrupt	R/W
Ch. 4	0x0840	Dynamic Status	R	**Ch. 10**	0x08A0	Dynamic Status	R
	0x0844	Latched Status	R/W		0x08A4	Latched Status	R/W
	0x0848	Interrupt Enable	R/W		0x08A8	Interrupt Enable	R/W
	0x084C	Set Edge/Level Interrupt	R/W		0x08AC	Set Edge/Level Interrupt	R/W
Ch. 5	0x0850	Dynamic Status	R	**Ch. 11**	0x08B0	Dynamic Status	R
	0x0854	Latched Status	R/W		0x08B4	Latched Status	R/W
	0x0858	Interrupt Enable	R/W		0x08B8	Interrupt Enable	R/W
	0x085C	Set Edge/Level Interrupt	R/W		0x08BC	Set Edge/Level Interrupt	R/W
Ch. 6	0x0860	Dynamic Status	R	**Ch. 12**	0x08C0	Dynamic Status	R
	0x0864	Latched Status	R/W		0x08C4	Latched Status	R/W
	0x0868	Interrupt Enable	R/W		0x08C8	Interrupt Enable	R/W
	0x086C	Set Edge/Level Interrupt	R/W		0x08CC	Set Edge/Level Interrupt	R/W

Overcurrent

0x0910	Dynamic Status	R
0x0914	Latched Status	R/W
0x0918	Interrupt Enable	R/W
0x091C	Set Edge/Level Interrupt	R/W

NAI Cares

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Status and Interrupts

MODULE MANUAL

Revision History

Revision	Revision Date	Description	Author
A	6/17/2019	Initial release	GC
A1	4/22/2020	ECO C07519: Module manuals updated for formatting consistency. No technical or specification updates.	MC

Table of Contents

1 Status and Interrupts

Status registers indicate the detection of faults or events. The status registers can be channel bit-mapped or event bit-mapped. An example of a channel bit-mapped register is the BIT status register, and an example of an event bit-mapped register is the FIFO status register.

For those status registers that allow interrupts to be generated upon the detection of the fault or the event, there are four registers associated with each status: *Dynamic, Latched, Interrupt Enabled*, and *Set Edge/Level Interrupt*.

Dynamic Status: The *Dynamic Status* register indicates the *current* condition of the fault or the event. If the fault or the event is momentary, the contents in this register will be clear when the fault or the event goes away. The *Dynamic Status* register can be polled, however, if the fault or the event is sporadic, it is possible for the indication of the fault or the event to be missed.

Latched Status: The *Latched Status* register indicates whether the fault or the event *has occurred* and keeps the state until it is cleared by the user. Reading the *Latched Status* register is a better alternative to polling the *Dynamic Status* register because the contents of this register will not clear until the user commands to clear the specific bit(s) associated with the fault or the event in the *Latched Status* register. Once the status register has been read, the act of writing a **1** back to the applicable status register to any specific bit (channel/event) location will "clear" the bit (set the bit to **0**). When clearing the channel/event bits, it is strongly recommended to write back the same bit pattern as read from the *Latched Status* register. For example, if the channel bit-mapped *Latched Status* register contains the value 0x0000 0005, which indicates fault/event detection on channel 1 and 3, write the value 0x0000 0005 to the *Latched Status* register to clear the fault/event status for channel 1 and 3. Writing a "1" to other channels that are not set (example 0x0000 000F) may result in incorrectly "clearing" incoming faults/events for those channels (example, channel 2 and 4).

Interrupt Enable: If interrupts are preferred upon the detection of a fault or an event, enable the specific channel/event interrupt in the *Interrupt Enable* register. The bits in *Interrupt Enable* register map to the same bits in the *Latched Status* register. When a fault or event occurs, an interrupt will be fired. Subsequent interrupts will not trigger until the application acknowledges the fired interrupt by clearing the associated channel/event bit in the *Latched Status* register. If the interruptible condition is still persistent after clearing the bit, this may retrigger the interrupt depending on the *Edge/Level* setting.

Set Edge/Level Interrupt: When interrupts are enabled, the condition on retriggering the interrupt after the Latch Register is "cleared" can be specified as "edge" triggered or "level" triggered. Note, the Edge/Level Trigger also affects how the Latched Register value is adjusted after it is "cleared" (see 1.1.1).

- *Edge triggered*: An interrupt will be retriggered when the Latched Status register change from low (0) to high (1) state. Uses for edge-triggered interrupts would include transition detections (Low-to-High transitions, High-to-Low transitions) or fault detections. After "clearing" an interrupt, another interrupt will not occur until the next transition or the re-occurrence of the fault again.
- *Level triggered*: An interrupt will be generated when the Latched Status register remains at the high (1) state. Level-triggered interrupts are used to indicate that something needs attention.

1.1 Interrupt Vector and Steering

When interrupts are enabled, the interrupt vector associated with the specific interrupt can be programmed with a unique number/identifier defined by the user such that it can be utilized in the Interrupt Service Routine (ISR) to identify the type of interrupt. When an interrupt occurs, the contents of the Interrupt Vector registers is reported as part of the interrupt mechanism. In addition to specifying the interrupt vector, the interrupt can be directed ("steered") to the native bus or to the application running on the onboard ARM processor.

1.2 Interrupt Trigger Types

In most applications, limiting the number of interrupts generated is preferred as interrupts are costly, thus choosing the correct Edge/Level interrupt trigger to use is important.

Example 1: Fault detection

This example illustrates interrupt considerations when detecting a fault like an “open” on a line. When an “open” is detected, the system will receive an interrupt. If the “open” on the line is persistent and the trigger is set to “edge”, upon “clearing” the interrupt, the system will not re-generate another interrupt. If, instead, the trigger is set to “level”, upon “clearing” the interrupt, the system will re-generate another interrupt. Thus, in this case, it will be better to set the trigger type to “edge”.

Example 2: Threshold detection

This example illustrates interrupt considerations when detecting an event like reaching or exceeding the “high watermark” threshold value. In a communication device, when the number of elements received in the FIFO reaches the high-watermark threshold, an interrupt will be generated. Normally, the application would read the count of the number of elements in the FIFO and read this number of elements from the FIFO. After reading the FIFO data, the application would “clear” the interrupt. If the trigger type is set to “edge”, another interrupt will be generated only if the number of elements in FIFO goes below the “high watermark” after the “clearing” the interrupt and then fills up to reach the “high watermark” threshold value. Since receiving communication data is inherently asynchronous, it is possible that data can continue to fill the FIFO as the application is pulling data off the FIFO. If, at the time the interrupt is “cleared”, the number of elements in the FIFO is at or above the “high watermark”, no interrupts will be generated. In this case, it will be better to set the trigger type to “level”, as the purpose here is to make sure that the FIFO is serviced when the number of elements exceeds the high watermark threshold value. Thus, upon “clearing” the interrupt, if the number of elements in the FIFO is at or above the “high watermark” threshold value, another interrupt will be generated indicating that the FIFO needs to be serviced.

1.3 Dynamic and Latched Status Registers Examples

The examples in this section illustrate the differences in behavior of the Dynamic Status and Latched Status registers as well as the differences in behavior of Edge/Level Trigger when the Latched Status register is cleared.

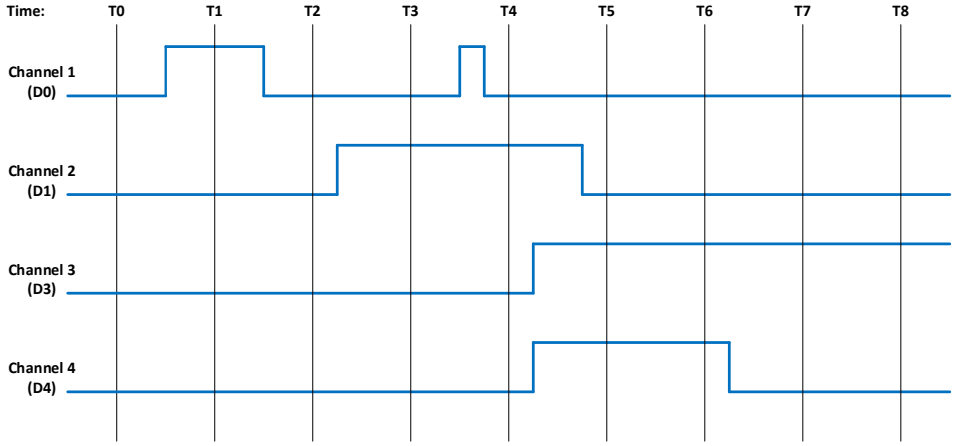

Figure 1 - Example of Module's Channel-Mapped Dynamic and Latched Status States

Time	Dynamic Status	No Clearing of Latched Status	Clearing of Latched Status (Edge-Triggered)		Clearing of Latched Status (Level-Triggered)	
		Latched Status	Action	Latched Status	Action	Latched
T0	0x0	0x0	Read Latched Register	0x0	Read Latched Register	0x0
T1	0x1	0x1	Read Latched Register	0x1		0x1
			Write 0x1 to Latched Register		Write 0x1 to Latched Register	
				0x0		*0x1*
T2	0x0	0x1	Read Latched Register	0x0	Read Latched Register	0x1
					Write 0x1 to Latched Register	
						0x0
T3	0x2	0x3	Read Latched Register	0x2	Read Latched Register	0x2
			Write 0x2 to Latched Register		Write 0x2 to Latched Register	
				0x0		*0x2*
T4	0x2	0x3	Read Latched Register	0x1	Read Latched Register	0x3
			Write 0x1 to Latched Register		Write 0x3 to Latched Register	
				0x0		*0x2*
T5	0xC	0xF	Read Latched Register	0xC	Read Latched Register	0xE
			Write 0xC to Latched Register		Write 0xE to Latched Register	
				0x0		*0xC*
T6	0xC	0xF	Read Latched Register	0x0	Read Latched Register	0xC
					Write 0xC to Latched Register	
						0xC
T7	0x4	0xF	Read Latched Register	0x0	Read Latched Register	0xC
					Write 0xC to Latched Register	
						0x4
T8	0x4	0xF	Read Latched Register	0x0	Read Latched Register	0x4

1.4 Interrupt Examples

The examples in this section illustrate the interrupt behavior with Edge/Level Trigger.

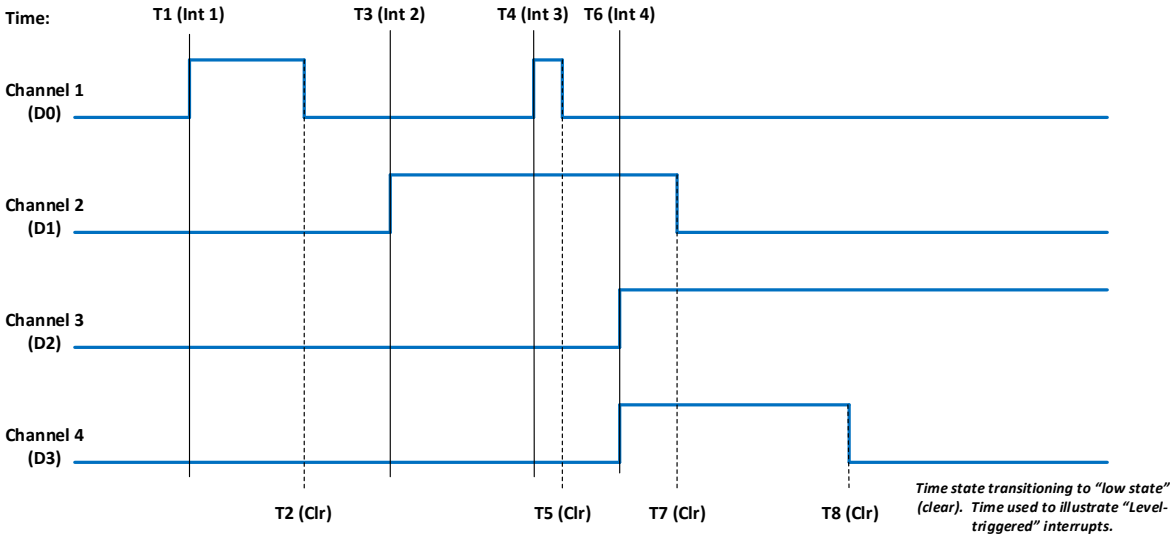

Figure 2 - Illustration of Latched Status State for Module with 4-Channels with Interrupt Enabled

Time	Latched Status (Edge-Triggered – Clear Multi-Channel) Action	Latched	Latched Status (Edge-Triggered – Clear Single Channel) Action	Latched	Latched Status (Level-Triggered – Clear Multi-Channel) Action	Latched
T1 (Int 1)	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x1
	Write 0x1 to Latched Register		Write 0x1 to Latched Register		Write 0x1 to Latched Register	
		0x0		*0x0*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear until T2.	*0x1*
T3 (Int 2)	**Interrupt Generated** Read Latched Registers	0x2	**Interrupt Generated** Read Latched Registers	0x2	**Interrupt Generated** Read Latched Registers	0x2
	Write 0x2 to Latched Register		Write 0x2 to Latched Register		Write 0x2 to Latched Register	
		0x0		*0x0*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear until T7.	*0x2*
T4 (Int 3)	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x3
	Write 0x1 to Latched Register		Write 0x1 to Latched Register		Write 0x3 to Latched Register	
		0x0		*0x0*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0x3 is reported in Latched Register until T5.	*0x3*
					Interrupt re-triggers Note, interrupt re-triggers after each clear until T7.	*0x2*

T6 (Int 4)	**Interrupt Generated** Read Latched Registers	0xC	**Interrupt Generated** Read Latched Registers	0xC	**Interrupt Generated** Read Latched Registers	0xE
	Write 0xC to Latched Register		Write 0x4 to Latched Register		Write 0xE to Latched Register	
		0x0	***Interrupt re-triggers*** Write 0x8 to Latched Register	*0x8*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0xE is reported in Latched Register until T7.	*0xE*
				0x0	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0xC is reported in Latched Register until T8.	*0xC*
					Interrupt re-triggers Note, interrupt re-triggers after each clear and 0x4 is reported in Latched Register always.	*0x4*

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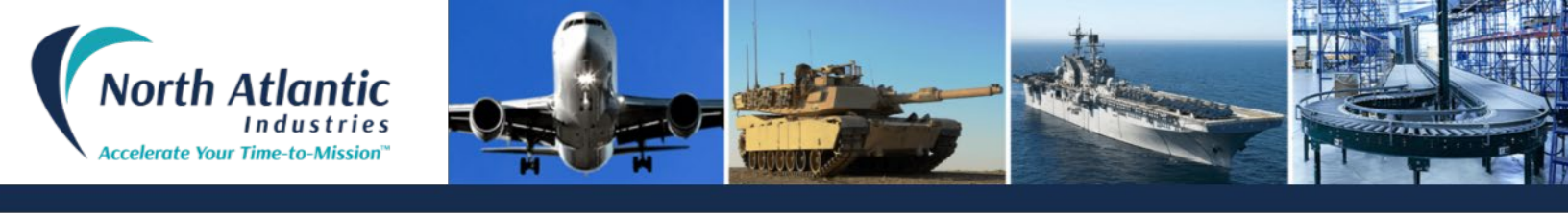

User Watchdog Timer

MODULE MANUAL
APPENDIX

Revision History

Revision	Revision Date	Description	Draft/Apprv.
A	6/25/2019	Initial release	GC
A1	10/7/2019	Appended “User” to Watchdog Timer to indicate that the Watchdog Timer is controlled by the user’s application.	GC
A2	4/22/2020	ECO C07519: Module manuals updated for formatting consistency. No technical or specification updates.	MC
B	3/29/2021	ECO C08381: Re-identified Digital-to-Synchro/Resolver (D/S) or Digital-to-L(R)VDT (D/LV) Modules are currently unsupported (at this time).	ARS

Table of Contents

1 User Watchdog Timer Module Manual

1.1 User Watchdog Timer Capability

The User Watchdog Timer (UWDT) Capability is available on the following modules:

- AC Reference Source Modules
  - AC1 – 1 Channel, 2-115 Vrms, 47 Hz – 20kHz
  - AC2 – 2 Channels, 2-28 Vrms, 47 Hz – 20kHz
  - AC3 – 1 Channel, 28-115 Vrms, 47 Hz – 2.5 kHz
- Differential Transceiver Modules
  - DF1/DF2 – 16 Channels Differential I/O
- Digital-to-Analog (D/A) Modules
  - DA1 – 12 Channels, ±10 VDC @ 25 mA, Voltage or Current Control Modes
  - DA2 – 16 Channels, ±10 VDC @ 10 mA
  - DA3 – 4 Channels, ±40 VDC @ ±100 mA, Voltage or Current Control Modes
  - DA4 – 4 Channels, ±80 VDC @ 10 mA
  - DA5 - 4 Channels, ±65 VDC or ±2 A, Voltage or Current Control Modes
- Digital-to-Synchro/Resolver (D/S) or Digital-to-L(R)VDT (D/LV) Modules

  (Not supported)
- Discrete I/O Modules
  - DT1/DT4 – 24 Channels, Programmable for either input or output, output up to 500 mA per channel from an applied external 3 – 60 VCC source.
  - DT2/DT5 – 16 Channels, Programmable for either input voltage measurements (±80 V) or as a bi-directional current switch (up to 500 mA per channel).
  - DT3/DT6 – 4 Channels, Programmable for either input voltage measurements (±100 V) or as a bi-directional current switch (up to 3 A per channel).
- TTL/CMOS Modules
  - TL1-TL8 – 24 Channels, Programmable for either input or output.

1.2 Principle of Operation

The User Watchdog Timer is optionally activated by the applications that require the module's outputs to be disabled as a failsafe in the event of an application failure or crash. The circuit is designed such that a specific periodic write strobe pattern must be executed by the software to maintain operation and prevent the disablement from taking place.

The User Watchdog Timer is inactive until the application sends an initial strobe by writing the value 0x55AA to the *UWDT Strobe* register. After activating the User Watchdog Timer, the application must continually strobe the timer within the intervals specified with the configurable *UWDT Quiet Time* and *UWDT Window* registers. The timing of the strobes must be consistent with the following rules:

- The application must not strobe during the Quiet time.
- The application must strobe within the Window time.
- The application must not strobe more than once in a single window time.

A violation of any of these rules will trigger a User Watchdog Timer fault and result in shutting down any isolated power supplies and/or disabling any active drive outputs, as applicable for the specific module. Upon a User Watchdog Timer event, recovery to the module shutting down will require the module to be reset.

The Figure 1 and Figure 2 provides an overview and an example with actual values for the User Watchdog Timer Strobes, Quiet Time and Window. As depicted in the diagrams, there are two processes that run in parallel. The Strobe event starts the timer for the beginning of the "Quiet Time". The timer for the Previous Strobe event continues to run to ensure that no additional Strobes are received within the "Window" associated with the Previous Strobe.

The optimal target for the user watchdog strobes should be at the interval of [Quiet time + ½ Window time] after the previous strobe, which will place the strobe in the center of the window. This affords the greatest margin of safety against unintended disablement in critical operations.

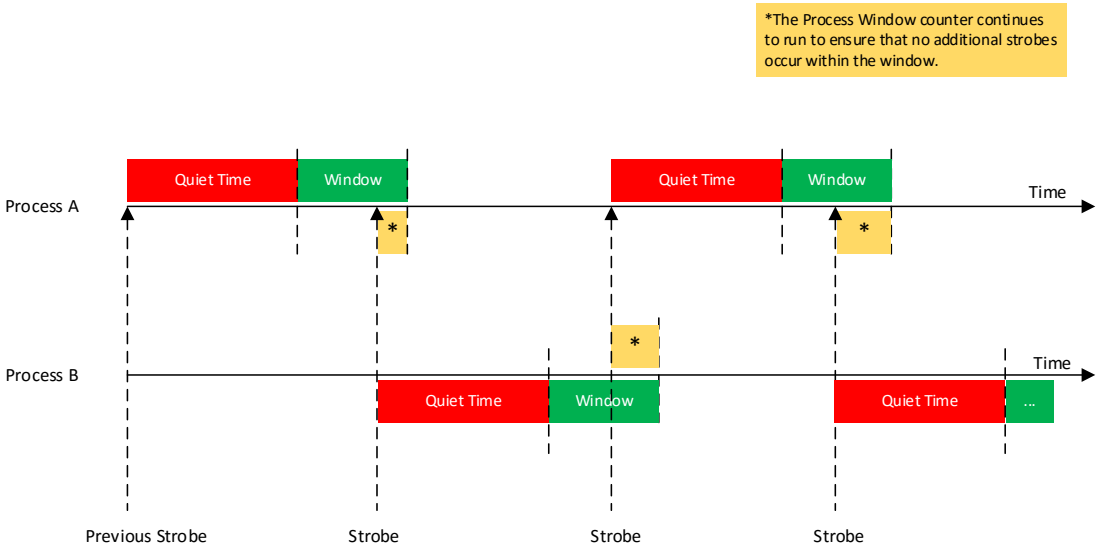

Figure 1 – User Watchdog Timer Overview

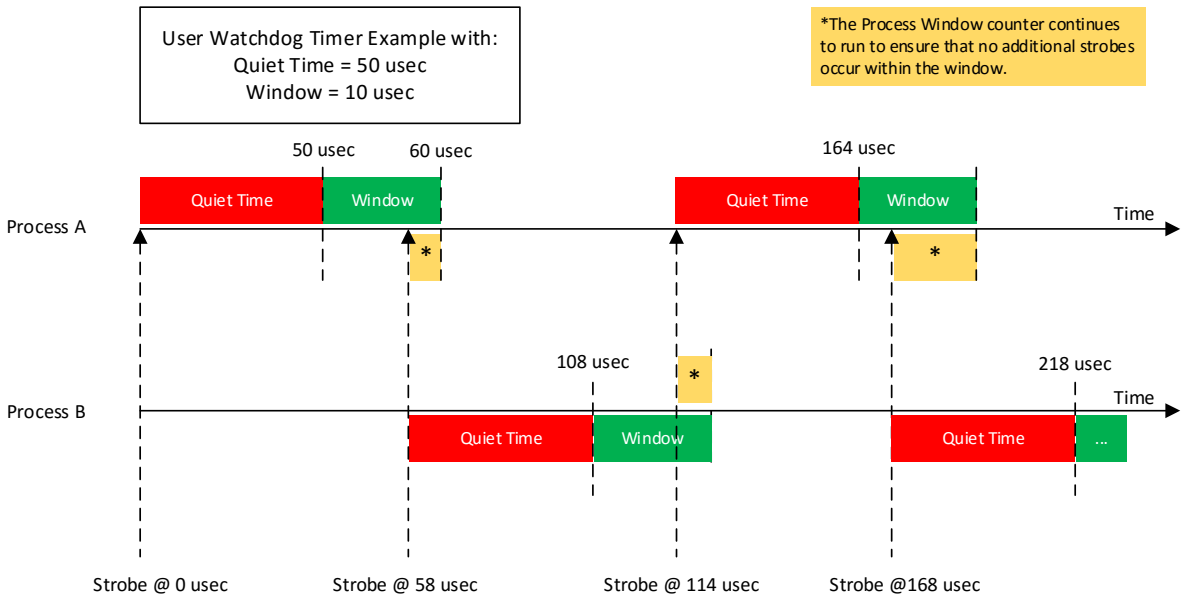

Figure 2 – User Watchdog Timer Example

Figure 3 illustrates examples of User Watchdog Timer failures.

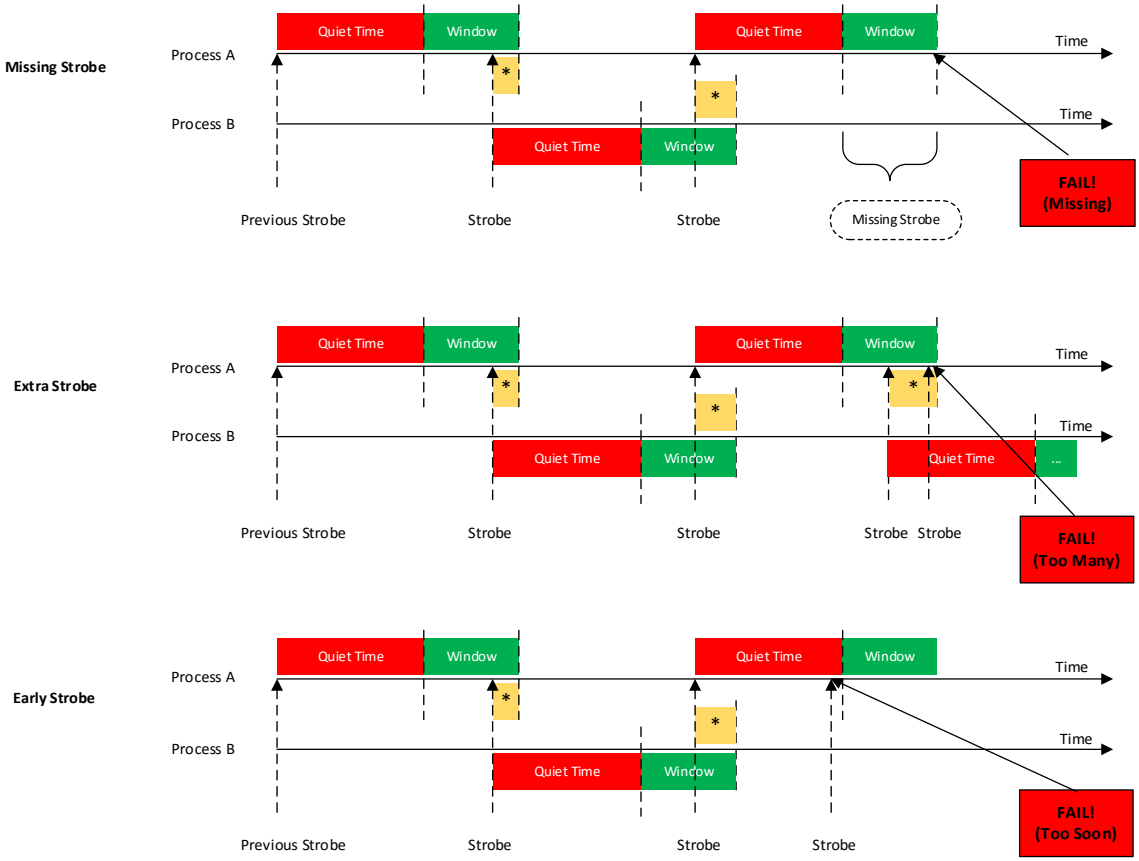

Figure 3 – User Watchdog Timer Failures

1.3 Register Descriptions

The register descriptions provide the register name, Type, Data Range, Read or Write information, Initialized Value, and a description of the function.

1.3.1 User Watchdog Timer Registers

The registers associated with the User Watchdog Timer provide the ability to specify the *UWDT Quiet Time* and the *UWDT Window* that will be monitored to ensure that EXACTLY ONE User Watchdog Timer (UWDT) Strobe is written within the window.

1.3.1.1 UWDT Quiet Time

Function: Sets Quiet Time value (in microseconds) to use for the User Watchdog Timer Frame.

Type: unsigned binary word (32-bit)

Data Range: 0 µsec to 2^32 µsec (0x0 to 0xFFFFFFFF)

Read/Write: R/W

Initialized Value: 0x0

Operational Settings: LSB = 1 µsec. The application must NOT write a strobe in the time between the previous strobe and the end of the Quiet time interval. In addition, the application must write in the *UWDT Window* EXACTLY ONCE.

1.3.1.2 UWDT Window

Function: Sets Window value (in microseconds) to use for the User Watchdog Timer Frame.

Type: unsigned binary word (32-bit)

Data Range: 0 µsec to 2^32 µsec (0x0 to 0xFFFFFFFF)

Read/Write: R/W

Initialized Value: 0x0

Operational Settings: LSB = 1 µsec. The application must write the strobe once within the Window time after the end of the Quiet time interval. The application must write in the *UWDT Window* EXACTLY ONCE.

This setting must be initialized to a non-zero value for operation and should allow sufficient tolerance for strobe timing by the application.

1.3.1.3 UWDT Strobe

Function: Writes the strobe value to be use for the User Watchdog Timer Frame.

Type: unsigned binary word (32-bit)

Data Range: 0x55AA

Read/Write: W

Initialized Value: 0x0

Operational Settings: At startup, the user watchdog is disabled. Write the value of 0x55AA to this register to start the user watchdog timer monitoring after initial power on or a reset. To prevent a disablement, the application must periodically write the strobe based on the user watchdog timer rules.

1.3.2 Status and Interrupt

The modules that are capable of User Watchdog Timer support provide status registers for the User Watchdog Timer.

1.3.2.1 User Watchdog Timer Status

The status register that contains the User Watchdog Timer Fault information is also used to indicate channel Inter-FPGA failures on modules that have communication between FPGA components. There are four registers associated with the User Watchdog Timer Fault/Inter-FPGA Failure Status: *Dynamic, Latched, Interrupt Enable,* and *Set Edge/Level Interrupt*.

User Watchdog Timer Fault/Inter-FPGA Failure Dynamic Status		
User Watchdog Timer Fault/Inter-FPGA Failure Latched Status		
User Watchdog Timer Fault/Inter-FPGA Failure Interrupt Enable		
User Watchdog Timer Fault/Inter-FPGA Failure Set Edge/Level Interrupt		
Bit(s)	**Status**	**Description**
D31	User Watchdog Timer Fault Status	**0** = No Fault **1** = User Watchdog Timer Fault
D30:D0	Reserved for Inter-FPGA Failure Status	Channel bit-mapped indicating channel inter-FPGA communication failure detection.

Function: Sets the corresponding bit (D31) associated with the channel's User Watchdog Timer Fault error.
Type: unsigned binary word (32-bit)
Data Range: 0x0000 0000 to 0xFFFF FFFF
Read/Write: R (*Dynamic*), R/W (*Latched*, *Interrupt Enable*, *Edge/Level Interrupt*)
Initialized Value: 0

1.3.2.2 Interrupt Vector and Steering

When interrupts are enabled, the interrupt vector associated with the specific interrupt can be programmed (typically with a unique number/identifier) such that it can be utilized in the Interrupt Service Routine (ISR) to identify the type of interrupt. When an interrupt occurs, the contents of the Interrupt Vector registers is reported as part of the interrupt mechanism.

In addition to specifying the interrupt vector, the interrupt can be directed ("steered") to the native bus or to the application running on the onboard ARM processor.

Note, the Interrupt Vector and Interrupt Steering registers are mapped to the Motherboard Common Memory and these registers are associated with the Module Slot position (refer to Function Register Map).

1.3.2.3 Interrupt Vector

Function: Set an identifier for the interrupt.
Type: unsigned binary word (32-bit)
Data Range: 0x0000 0000 to 0xFFFF FFFF
Read/Write: R/W
Initialized Value: 0
Operational Settings: When an interrupt occurs, this value is reported as part of the interrupt mechanism.

1.3.2.4 Interrupt Steering

Function: Sets where to direct the interrupt.
Type: unsigned binary word (32-bit)
Data Range: See table
Read/Write: R/W
Initialized Value: 0
Operational Settings: When an interrupt occurs, the interrupt is sent as specified:

Direct Interrupt to VME	1
Direct Interrupt to ARM Processor (via SerDes) *(Custom App on ARM or NAI Ethernet Listener App)*	2
Direct Interrupt to PCIe Bus	5
Direct Interrupt to cPCI Bus	6

1.3.3 Function Register Map

Key: ***Bold Italic = Configuration/Control***

Bold Underline = Status

*When an event is detected, the bit associated with the event is set in this register and will remain set until the user clears the event bit. Clearing the bit requires writing a 1 back to the specific bit that was set when read (i.e. write-1-to-clear, writing a '1' to a bit set to '1' will set the bit to '0').

1.3.3.1 User Watchdog Timer Registers

0x01C0	***UWDT Quiet Time***	R/W
0x01C4	***UWDT Window***	R/W
0x01C8	***UWDT Strobe***	W

1.3.3.2 Status Registers

User Watchdog Timer Fault/Inter-FPGA Failure

0x09B0	**Dynamic Status**	R
0x09B4	**Latched Status***	R/W
0x09B8	***Interrupt Enable***	R/W
0x09BC	***Set Edge/Level Interrupt***	R/W

1.3.3.3 Interrupt Register

The Interrupt Vector and Interrupt Steering registers are mapped to the Motherboard Memory Space and these addresses are absolute based on the module slot position. In other words, do not apply the Module Address offset to these addresses.

0x056C	***Module 1 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x066C	***Module 1 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x076C	***Module 2 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x086C	***Module 2 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x096C	***Module 3 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0A6C	***Module 3 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0B6C	***Module 4 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0C6C	***Module 4 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0D6C	***Module 5 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0E6C	***Module 5 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0F6C	***Module 6 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x106C	***Module 6 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W

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